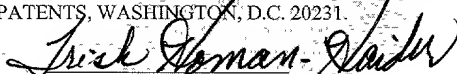# APPLICATION FOR LETTERS PATENT

FOR

CIRCUIT AND METHOD FOR TEST AND REPAIR

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CIRCUIT AND METHOD FOR TEST AND REPAIR

Technical Field

[0001]   The present invention relates generally to the computer memory field and, more specifically, to test and repair of memory.

Background of the Invention

[0002]   A memory device is often produced using a semiconductor fabrication process. In the current application, the term "semiconductor" will be understood to mean any semiconductor material, including but not limited to bulk semiconductive materials (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). Moreover, it shall be understood that a semiconductor device may comprise conductive and insulative materials as well as a semiconductive material. The result of a semiconductor process may be a die comprising memory circuitry, and it may be desirable to test that circuitry at some point during the process of constructing a memory device comprising that die. For instance, testing may occur while the die is part of a semiconductor wafer, after singulation from the wafer, during die packaging, or once the memory device (chip) is completed.

[0003]   One conventional method of testing such a chip is to have an external testing device write data to every memory cell of the chip, then read data from every memory cell, and compare the input with the output. Such a comparison may reveal cells that failed to store the data properly. The addresses corresponding to these defective cells can be stored by the external testing device, and that stored data may be used to repair the chip. In order to effect such repair, redundant cells are provided on the chip, as well as at least one bank of fuses or anti-fuses that controls access to the redundant cells. Assuming the bank to be comprised of anti-fuses, repair circuitry receives each address corresponding to a defective cell and, based on that address, blows at least

one anti-fuse, thereby isolating the defective cell and associating the address with a redundant cell.

[0004]   This error detect and repair scheme, however, raises issues. One such issue is the number of chips that may be tested at one time. A typical testing device is an AMBYX machine which can hold 256 chips. However, for cost reasons, the AMBYX has only 64 terminals (known as "DQ's") for reading from and writing to the chips. As a result, the chips must share these DQ resources. Assuming each chip has only four DQ's of its own (in which case the chips would be known as a "x4" part), then the AMBYX could access only 16 chips at one time. Thus a typical testing process would involve writing data to cells of 16 chips; reading data from cells of all 16 chips; comparing the written data with the read data; and, for cells wherein the written data and read data do not match, storing the addresses of those failed cells. These steps must be performed 15 more times in order to test all 256 chips on the AMBYX. Moreover, once repaired, the chips are often retested in a second test cycle to determine whether the repair was successful, thereby requiring even more time, especially if the chips must be removed from the AMBYX for repair and then placed back onto the AMBYX for retesting. Further, more than one type of test is often conducted. As a result, there is a desire in the art to shorten test time.

Summary of the Invention

[0005]   Accordingly, exemplary embodiments of the current invention provide methods and circuitry for testing and repairing a chip. In one exemplary embodiment, data stored on a chip's memory is read to the extent that it is accessed from the memory array. However, rather than transmit the data to an external testing device, the chip's output circuitry is tri-stated, the external testing device transmits to the chip the data that is expected to be stored, and a comparison between the stored data and the expect data occurs on chip.

[0006]   In another embodiment, a result of a test, be it one described above or another, are stored on the chip. In a preferred embodiment, at most one failed address is

stored, along with a bit indicating that a failure has been found. In a more preferred embodiment, the stored address is the last failed address resulting from the test; and only the column address, rather than both the column and row address, is stored. In another embodiment, the register of a failed part is cleared after testing, and further testing commences. If such testing reveals a failed address already associated with a redundant cell, that address is not stored, although a bit indicating that a failure has been found is stored.

[0007] In yet another embodiment, chip repair is carried out wherein, given a defective memory cell, an entire group of memory cells including the defective cell is replaced by a redundant group of cells. In a preferred embodiment of this type, an entire column of redundant memory cells replaces a column of memory cells containing the defective cell. In a more preferred embodiment, the address of the defective memory cell is stored in an on-chip register. In an even more preferred embodiment, only one column -- the column including the last recorded failed memory cell -- is replaced as a result of one test cycle.

[0008] These and other embodiments within the scope of the invention include within the scope both apparatuses and methods; and still other embodiments encompass combinations of the embodiments listed above.

Brief Description of the Drawings

[0009] FIG. 1 depicts a prior art testing device for a plurality of chips.

[0010] FIG. 2 is a table comparing a test method known in the art with an exemplary method within the scope of the current invention.

[0011] FIG. 3 illustrates circuitry of an exemplary apparatus embodiment within the scope of the current invention.

[0012] FIG. 4 is a table comparing a second test method known in the art with a second exemplary method within the scope of the current invention.

[0013] FIG. 5 is a table comparing a third test method known in the art with a third exemplary method within the scope of the current invention.

[0014]   FIG. 6 depicts another exemplary apparatus embodiment within the scope of the current invention.

Detailed Description of the Preferred Embodiments

[0015]   In terms of error detection, exemplary embodiments of the current invention shorten test time by presenting a testing scheme alternative to the one presented in the Background. To begin with, a simplified test method practiced in the prior art is presented. FIG. 1 presents a portion of a simplified tester 900 having only four DQ's 902. While the tester 900 may be able to physically hold 16 chips (A-P), its circuitry is designed to direct signals to and from at most four chips at one time. It is understood that the tester 900 also has conductive lines (not shown) that carry address and command information to the chips, and that these lines are also limited in number and so can direct signals to and from at most four chips at a time. The areas in which the tester may communicate in such a fashion are identified in this specification as "regions." Tester 900 has four regions 904, 906, 908, and 910. Further, it is assumed for purposes of explanation that the parts A-P are "x1" parts (each having only one DQ) and have only four memory addresses.

[0016]   The prior art commands for one exemplary test using tester 900 are depicted in the left-hand column of the table in FIG. 2. During the first clock cycle, the same bit is written to a cell corresponding to the first address in each of chips A-D. Because the same bit is being written, the write step may occur in parallel with respect to chips A-D. Similar parallel writing steps may be taken to write to the second, third, and fourth addresses of chips A-D. As a result, writing to every address of all four chips requires 4 clock cycles. However, reading from the chips A-D for purposes of off-chip comparison with expected data may not be performed in parallel, as the chips may not output identical data due to chip failures which this test seeks to reveal. As a result, the tester must read from each address in each chip in series. Table 1 indicates that reading from all four addresses of chip A requires four clock

cycles (5-8). In fact, four clock cycles are required to read from all addresses of each chip, resulting in a total of twenty clock cycles needed to test the four chips 20 in this one region 904 of the tester 900. An additional 20 clock cycles is then needed for each of the remaining regions 906, 908, 910. Thus in this example, test time takes 80 clock cycles, and that amount is just for one test. Generally several tests are performed on the chips, with each test requiring 80 clock cycles. Moreover, chips that failed a test the first time often repeat that test after being repaired, thereby requiring even more test time. One can now appreciate the degree to which the required test time can multiply.

[0017]   At least one exemplary embodiment of the current invention affects the time required to perform such a test. Such an embodiment is depicted in FIG. 3, which illustrates a semiconductor die as part of a chip 10 and a DQ 12 of a tester. Chip 10 includes a memory array 14; an address latch 15 that is configured to transmit a memory address (and may further comprise a separate row address latch and column address latch); an anti-fuse bank 40 which, based on its programming state, may divert a signal for a cell in the memory array to one of the redundant memory cells 42; and output circuitry 16. The output circuitry 16 is connected to the memory array 14 and the DQ 12. Output circuitry 16 comprises four transistors 18, 20, 22, and 24. The gates of p-channel transistor 18 and n-channel transistor 20 are connected to each other and to the memory array 14. Their drains are also connected to each other and to DQ 12. N-channel transistor 22 is coupled to ground and to transistor 20 and is driven by a signal ENABLE. A complementary signal ENABLE* drives transistor 24, which is coupled to a voltage source Vcc and to transistor 18.

[0018]   In a standard read operation, the ENABLE signal represents a high voltage signal that turns on transistor 22. Accordingly, the ENABLE* signal represents a low voltage signal that turns on transistor 24. A data value from at least one cell in memory array 14 (designated by the address in the address latch 15) is transmitted to the gates of transistors 18 and 20, and an inverted signal is output from their drains to the DQ 12. However, in a test mode under an exemplary embodiment of the current invention, ENABLE is at low voltage. As a result, transistor 22 turns off (isolating

the output circuitry 16 from ground), ENABLE* is at a high voltage, and transistor 24 turns off (isolating the output circuitry 16 from Vcc). The state of the output circuitry 16 in this mode is known as a "tri-state." The data value from memory cell 14 nevertheless transmits to an on-chip comparison circuit 26, which, in this example, is an exclusive NOR gate 28 that receives both the data from the memory array 14 and the data transmitted from the tester's DQ 12 (it is preferred, although not required, that the signal from DQ 12 first pass through an input buffer 30). Although the output circuitry 16 has been tri-stated and data is being transmitted to the chip 10 through the DQ 12, the chip 10 is considered to be in a "read" mode given that the data stored on chip 10 is being accessed. Based on the truth table for an EXCLUSIVE NOR operation, the EXCLUSIVE NOR gate 28 will output a low voltage signal only when both inputs fail to match, thereby indicating a defect in the cell corresponding to the memory address. The low voltage output from the EXCLUSIVE NOR gate prompts the register 32 to store the memory address transmitted by the address latch 15. Moreover, it is also preferable (although not required) for purposes of further testing as discussed below that the register 32 also store a bit that indicates whether an error has been found. For purposes of explaining other exemplary embodiments of the current invention, this bit will be referred to as the "fail flag."

[0019]   The right column of FIG. 2 illustrates that using the circuitry described above allows for an exemplary method of testing chips A-P on FIG. 1's tester 900 with fewer steps than was used in the prior art. As in the prior art, a particular bit may be written to every chip in a region in a parallel manner. Thus, writing to the first address of chips A-D can be performed in the same clock cycle, as can writing to the second, third, and fourth addresses. While writing to chips A-D takes the same number of clock cycles as in the prior art, the savings in this exemplary testing method appear when the chips enter their "read" mode.

[0020]   Unlike the prior art test, the tester's DQ's 902 are not needed to serially transmit possibly differing data *from* chips A-D. This is because analysis of the chips' stored data occurs within each chip. Thus, the tester's DQ's 902 may now be used to transmit *to* chips A-D the data that is expected to be stored in the first address

on those chips. Because the data written to the first address is the same for chips A-D, the expected data is also the same, and that expected data may be therefore transmitted by the tester in a parallel fashion. As a result, only one clock cycle is used to test the first address in chips A-D. A mismatch between the expected data and the data read from the first address of any of the chips A-D suggests a defective memory cell. In that event, the first address of the relevant chip would be stored in its register 32 along with data --such as the fail flag -- indicating that at least one error has been found on that chip.

[0021]   Subsequently, the second address of chips A-D is read during the next clock cycle and compared with the expected data, and so on for the third and fourth addresses, with the failed addresses being stored in the appropriate register 32 accordingly. As a result, this exemplary testing method accomplishes in eight clock cycles what it took the prior art twenty clock cycles to accomplish. Even after adding the preferred steps of serially reading for the fail flag that could result from the on-chip comparisons, clock cycle savings are still realized in comparison to the prior art method. It is further preferred that the circuit in FIG. 3 and process of FIG. 2 be implemented with chips that exhibit a latency of 1 or 2, wherein latency indicates the delay in the number of clock cycles between the arrival of a "read" command and the availability of data to be read.

[0022]   Moreover, it should be remembered that the example is a relatively simple one, with each chip having only four addresses and the tester 900 being able to test only four chips at once. As discussed in the background section, it is not unusual to test chips having millions of addresses per chip and to test them sixteen at a time. The savings offered by the exemplary method embodiment disclosed above become even greater with added complexity of the test scheme.

[0023]   For instance, assuming that chips A-P had five addresses rather than four, the table in FIG. 4 illustrates that the prior art test of region 904 would require five additional clock cycles: one clock cycle for a parallel write command to the fifth address of chips A-D; and four clock cycles, each needed to read from the fifth address of each chip A-D. In contrast, the exemplary method could use only two

additional clock cycles: one clock cycle for a parallel write command and one clock cycle for a parallel read command.

[0024]   Another example illustrated in the table of FIG. 5 assumes that five chips (each having four addresses) could be tested in parallel rather than four chips. The prior art method would require four more clock cycles to read from the four addresses of that extra part, whereas the exemplary method would require only one extra clock cycle to read the fail flag from the extra part; reading from all addresses of chip E requires no additional clock cycles, as that can be performed in the same clock cycle for reading from the other chips.

[0025]   As a result, one can now appreciate that an increase in the chips per region, the number of regions, the number of tests, or the number of bits per chip results in a multiplied amount of clock cycle savings during testing using exemplary embodiments of the current invention. Such savings can result in shorter test time or allow more time for other tests. In fact, testing directed by the inventor using exemplary embodiments of the current invention has demonstrated a reduction in test time by 45%.

[0026]   The preferred number of failed address to be stored in register 32 can be based on balancing the desire to fabricate as small a chip as possible with the desire to increase the likelihood of being able to keep track of all addresses corresponding to defective cells after one test cycle. The greater amount of on-chip test circuitry (including a large register capable of storing many failed addresses and the supporting logic circuitry), the more likely it is to ensure such ability. The cost, however, is that a great amount of die space may be devoted to that. Conversely, a lesser amount of on-chip test circuitry (including a register capable of storing few failed addresses and less supporting logic circuitry) allows for less die space to be devoted at the cost of some ability to keep track of all failed addresses after one test cycle. Such a balancing has been made concerning Synchronous Dynamic Random Access Memory (SDRAM) parts recently fabricated by Micron Technology, Inc., including part numbers MT48LC32M4A2 (an 8 Meg x 4 x 4 bank part), MT48LC16M8A2 (a 4 Meg x 8 x 4 bank part), MT48LC8M16A2 (a 2 Meg x 16 x 4 bank part), and MT48LC4M32B2 (a

1 Meg x 32 x 4 bank part). These parts incorporate many of the exemplary embodiments of the current invention. An analysis of the failed cells found on these parts during testing revealed that 90% of the failed chips can be fully repaired by replacing only one column containing at least one defective cell with a redundant column. As a result, these parts have a register that stores only a single failed address at one time (preferably in addition to the fail flag), and that address is only the column address, without the row address. Accordingly, a relatively small failed address register and related logic circuitry is provided on-chip. Further, it is preferred that the register store the latest failed address, clearing any former address that may have been stored.

[0027]   After the test, the chips containing defective cells may be repaired. Such chips will be identified by the presence of the fail flag value in the register 32 of relevant chips. Chips without the fail flag may bypass the repair process, thereby allowing the limited resources of the repair device to be devoted to the chips that need repair.

[0028]   Once the chips have been repaired, they may undergo a repeat of the previous test. Alternatively, they and the chips that passed the previous test may be subjected to a different test. In such cases, the address and fail-flag value may be cleared from the repaired chips' registers 32 before testing continues, and the testing process proceeds as described above. Further testing may reveal a defect concerning an address wherein the originally associated column of cells has already been isolated in favor of a redundant column as a result of a prior repair. In some exemplary embodiments of the current invention, it is not desirable to include circuitry designed to isolate a one redundant column in favor of a second. Thus, although not required in every embodiment of the current invention, it is preferable in certain exemplary embodiments to avoid storing a failed address in register 32 if that address is already associated with a redundant cell. The status of the anti-fuses in the anti-fuse bank 40 can be used to determine if such is the case. If such a failure occurs, however, it is desirable to record the existence of the failure by storing the fail flag in register 32.

Thus, if at the end of a test, the register 32 stores a fail flag with no address, that is an indication that a redundant cell has failed, and the chip may be handled accordingly.

[0029]   Exemplary embodiments of the current invention generally accommodate systems using memory, wherein the memory can include nonvolatile, static, or dynamic memory, and wherein the memory can be a discrete device, embedded in a chip with logic, or combined with other components to form a system on a chip. For example, FIG. 6 illustrates a computer system 32, wherein a microprocessor 34 transmits address, data, and control signals to a memory-containing device 36 such as one including but not limited to those described above. A system clock circuit 38 provides timing signals for the microprocessor 34.

[0030]   One skilled in the art can appreciate that, although specific embodiments of this invention have been described above for purposes of illustration, various modifications may be made without departing from the spirit and scope of the invention. For example, the error detection methods described above may occur at any stage of die singulation, including but not limited to states in which the chip's die is part of a wafer, integral with at least one other die yet separate from a wafer, or completely singulated from all other die. Further, the error detection methods may occur at any stage of packaging, ranging from a bare die to a fully packaged chip, although it is preferred to carry out testing methods of the current invention with a fully packaged chip. Error detection methods can occur on any device capable of handling the chip based on its state of singulation or packaging, including AMBYX and TERADYNE devices. Error detection methods can occur during a test, probe, or burn-in (including cold burn-in) process. Concerning the function in at least some exemplary embodiments of storing a single defective address, it is not required under all exemplary embodiments of the current invention to store the last failed address. Rather, the current invention includes within its scope embodiments wherein the first failed address and only the first failed address (if any) is stored. Moreover, at least some error detection methods of the current invention may be used in either compression or non-compression data transfer test modes. Accordingly, the invention is not limited except as stated in the claims.